MxC™200 Family Design Considerations

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Application Note 010

Introduction

In this application note we provide detailed information on the design considerations and configurations in which the MxC200 family of ICs can be operated. We also will discuss ways to improve/optimize the performance of this device in each configuration. The MxC200 family consists of five different products using the MuxCapacitor topology in different ways. Each device comprises up to three MuxCapacitor (or MuxCap) stages which can be configured in several ways to achieve different output voltages and circuit functions. A MuxCap is a proprietary charge pump cell that includes all the switches, control circuitry, and clocking to allow the designer to build highly efficient charge pump circuit blocks.

The topics discussed in this note are also mentioned or explained in the MxC200 family datasheets, and this application note is intended to be complementary to the datasheets.

The power that MxC200 can deliver and the efficiency depends on many factors including:

- The series and/or parallel configurations of the MuxCap stages
- The number as well as values of the flying and output capacitors
- The switching frequency
- The PCB layout
- The thermal resistance of the device package to the printed circuit board.

Each one of these topics is discussed in more detail in the following sections.

Different Configurations:

MxC200 family of integrated circuits with up to three MuxCapacitor© stages. One stage is rated for a maximum of 57V input for use with nominally 48V buses while two other stages are identical to each other and are rated for 30V max. When used as voltage dividers the voltage is reduced by half in each stage, and the available current increases by the inverse factor; i.e., the voltage is halved, and the current is doubled. As with a transformer using an AC voltage source, the MuxCap power is the same at the input and output, minus small efficiency losses. There are conversion losses in each stage due primarily to the Rdson or Drain to Source switch resistance, but these are small at lower currents and are primarily a factor at high currents. There are also AC switching losses, which are dependent on the operating frequency. Efficiencies of greater than 97% per stage are possible.

Another unique feature of the MuxCapacitor circuit is that is bidirectional, so if a voltage is applied to the “output”, the voltage is doubled at the “input”. This will be covered later.

Here we will present a brief description of the members of the MxC200 family of products. As mentioned above, there are five different products based on the MuxCap design and each has its own data sheet which should be referred to for more details.

- The 2D_048_015A is the original MxC200 with a nominal input voltage of 48V and 3 series connected MuxCap stages to get a total voltage reduction by a factor of eight. Each stage can be used to get a divide by 2, 4, and 8 to get 24V, 12V and 6V separately or a single output of 6V. The total output power for all the stages can be as high as 15W.
- The 2D_048_015B is intended for application that needs to provide a higher output current at 12V from a 48V source. This uses two 12V stages in parallel to get higher efficiency at 12V output voltage.
- The 2I_048_010A is intended for voltage isolated applications using the Helix CapIso™ technology and takes a 48V nominal input voltage and provides a pair of 24Vpp differential drivers to be used to capacitively transfer power to an isolated secondary load. This could be used with other members of the MxC200 family of products to provide various voltages for isolated circuitry. Details for these are in a separate document, "Using the MxC200 Family in Transformerless Isolated Applications".
- The 2U_012_010A is intended for applications where a voltage boost is required. An input voltage from 6V to 12V can be used to provide 24 or 48V nominal at the outputs.
- The 2D_24_010A is intended to be used primarily on the secondary side of a CapIso application to provide 48V, 12V and/or 6V from the isolated 24V provided by a 2I_048_010A differential driver device. It can also be used in non-isolated applications as well to provide those voltages

In an application, any combination of the stages could be used, with the stipulation that high voltage stage should always be connected to the highest input voltage. For applications with an input voltage less than 30V, the high voltage stage can be bypassed, and the input voltage can be connected to high voltage Vout1 and lower voltage stages directly. In such applications, the high voltage stage Cfly and Cin should still be populated even though the high voltage stage's output is not directly used. The reason for this is that Vin1/Vout1 (the names may vary depending on the specific family member) stage is used to power the gate drivers used in the other two lower voltage stages. The "Vout1" pin in this configuration becomes an input to the high voltage stage and should be connected to the stage 2 input so that the circuitry in the high voltage stage is powered up. Since the low voltage stages are identical, they could be used interchangeably.

The VINLDO input must be connected to a voltage source of 7V to 30V, so either the Vout1, Vout2, or Vout3 outputs can be used to power the internal LDO as long as their output is always greater than the VINLDO minimum of 7V. To maximize efficiency the VINLDO should connect to as low a source voltage as possible that will reliably supply the minimum 7V required source voltage. The VINLDO current requirement is approximately 1mA regardless what input voltage is used, so a lower source voltage will also mean less power will be consumed by the LDO. The LDO is the primary power loss at low output power levels.

The following discussions highlight some of the configurations in which the MxC200 family may be used.

Three Stages in Series (48V to 6V): 2D_048_015A

In this configuration if 48V is connected to the Vin1 input, 24V is generated at Vout1. When Vin2 is connected to Vout1 it uses Vout1 to generate 12V at Vout2. Likewise, stage 3's input connects to the output of stage 2 to provide 6V from stage 2's output. It should be noted that for a given amount of output power, the efficiency of a MuxCap stage is higher at higher input voltages. This is because for a given amount of output power, higher voltage corresponds to lower current and therefore the "I^2R" losses in the switches are less. When cascading stages, this results in lower efficiency because the power loss at each stage is multiplied by the loss in the previous stage(s). This higher I^2R loss is somewhat mitigated in the MxC200 family by the use of lower Rdson switches in the lower voltage stages. These losses are still relatively small compared to other methods of voltage conversion.

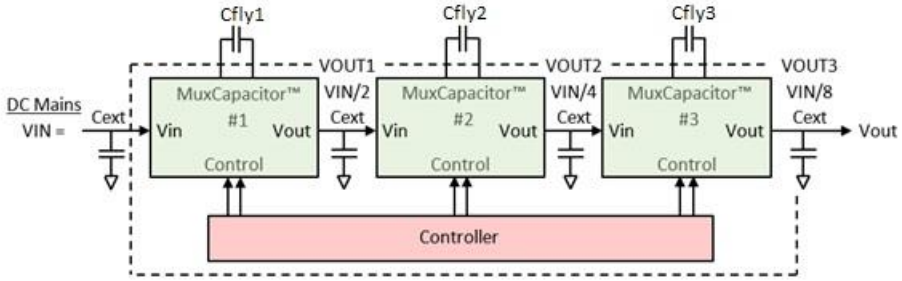

Figure 1. Series configuration of the 2D_048_015A for a divide by 8 solution

It is also possible to tap the intermediate voltages as well as the final output. This will reduce the current available to the following stage(s), but the total power available from all the stages will remain about the same.

Operation with low voltage stages in parallel powered from the high voltage stage (48V to 12V): 2D_048_015B

This is a divide-by-4 configuration shown in figure 2 and is very useful for converting a 48V bus to a 12V bus though it can be used for other input voltage levels such as converting 24V to 6V. Stages 2A and 2B are designed so they are 180 degrees out of phase with each other which minimizes the ripple. In this configuration there is minimal need for output capacitors since one or the other flying cap is virtually always connected in parallel with the output cap. This is OK for light loads, but higher power will still benefit from a larger output capacitor to premature current limiting and reduce ripple.

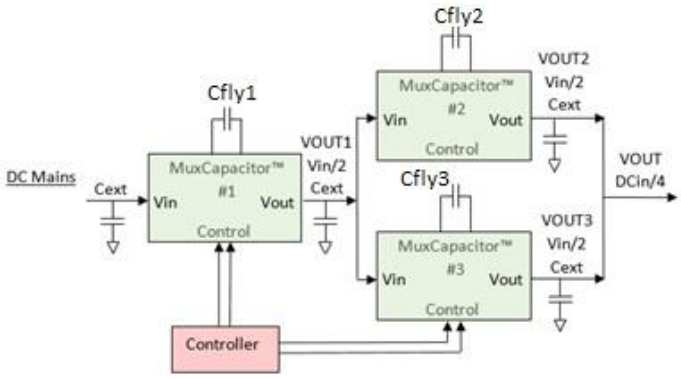

Figure 2. Divide-by-4 configuration the 2D_048_015B with stages 2 and 3 in parallel

If the maximum required output power is low, stage3 could be left disconnected and Cfly3 and Cout3 could be depopulated to reduce the parts count without significantly affecting the efficiency. Using both stages is parallel is most useful in higher power applications.

This configuration could be used in conjunction with a 12V-input Buck converter to provide a 48V to high efficiency point-of-load step-down solution.

Stages 2 and 3 in series and parallel (24V to 12V or 6V): 2D_024_010A

For input voltages lower than 30V, and only a divide-by-2 solution is required, it is more efficient to bypass stage1 and use stages 2 and 3 in parallel as shown in figure 3. As discussed previously, for this configuration, Cfly1 and Cin1 should still be populated with small capacitors, and the 2D_024_010A Vin1 should be connected to Vin2 which is also connected to the input power. Stage1 is now operated in reverse mode to generate the gate drive voltage which is required by stages 2 and 3 that drive the switches which are connected to the input voltage.

By connecting stages 2 and 3 in series, a divide by 2 and divide by 4 can be implemented in a similar way with the 2D_024_010A stage 1 input connected to the input supply and VINLDO connected to Vin or the stage 2 output. Keep in mind the voltage source for the internal LDO must remain above 7 volts, so if the Vin2 supply is less than about 14V (without a load) and the stage 2 output is the VINLDO source, the LDO source voltage could be compromised. The output voltage will sag slightly as a load is applied to either stage 2 or stage 3's output, and this could cause the LDO to drop out of regulation. In this case the input voltage should be used to power the VINLDO pin to assure a reliable voltage supply.

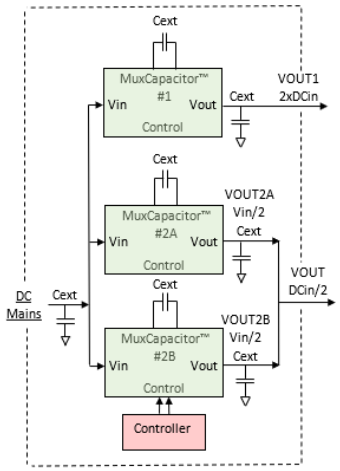

Figure 3. Parallel configuration of the 2D_024_010A with stages 2 and 3 providing a divide-by-2 solution for Vin<30V

Divide by two configuration (48V to 24V): 2D_048_015x

For input voltages above 30V and only a divide-by-2 function is required, use high voltage stage 1 alone. For this configuration stages 2 and 3 could be left unconnected and the Cfly and output caps for those stages can be depopulated.

For this configuration, the input of VINLDO would be connected to Vout1. Alternatively, to improve the efficiency of the LDO slightly (by 12mW) in a low current application, stage2 could be utilized to further reduce Vout1 and provide a lower voltage source for the LDO circuitry. In this case a small 0.1uF Cfly2 and Cout2 would be sufficient to provide the required current for the LDO, which is about 1mA. The net effect is to reduce the current from the power source at the cost of two small capacitors.

Multiplying voltage configurations (12V to 24V or 12V to 48V): 2U_012_010A

As has been alluded to previously, it is also possible to increase the voltage as a voltage multiplier. The 2U_012_010A MuxCapacitor charge pump operates as a voltage doubler or even quadrupler. As with the voltage reduction modes, the higher voltage stage 2, in this case, must be powered to generate the gate voltage levels for the lower voltage stages. Stage 2 must be more positive with respect to the output voltage of lower voltage stages even if high voltage stage 2's output is not being used and power is taken at the stage 1A/B outputs. If stage 1A and 1B inputs are connected to a 12V voltage input, Vin2 is connected to the Vout1A/B. Stage 2 will have 48V at Vout2. If 48V is not needed, the first stage output and Flying capacitor can be populated with a smaller capacitance.

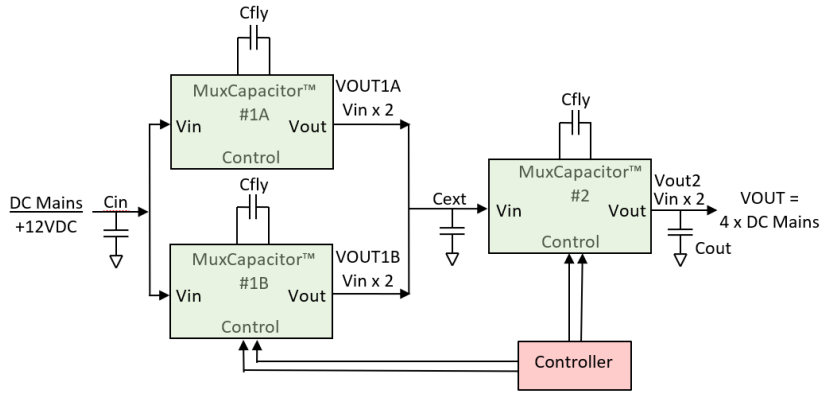

Figure 4. Configuration for using the 2U_012_010A voltage boost mode of operation

While with voltage reduction there is an increase in available current at each stage, in this case there is a reduction in current available as the voltage is increased. Efficiency is similar to or better than what is measured in the voltage reduction configurations. Even 6V inputs to the series connected stages 1A and1B could be used, but the efficiency and current ranges are lower. Do not apply voltages that will cause the output at Vout2 to be greater than the maximum recommended 57V or the output at Vout1A or 1B to be greater than 30 V.

Using the MxC Family to generate negative and/or regulated voltages:

Although the MxC200 Family does not natively generate negative voltages, it is quite simple to configure one of the flying capacitor inputs with two added diodes and two capacitors to get a negative source. By grounding the Vout2B pin, the Cfly top pin swings between the input stage voltage and ground. By AC coupling this signal to a series diode and a holding capacitor, a negative voltage can be generated as shown in figure 5. Any stage could be used, but in this example stage 2B is shown to generate -12V by filtering a 24Vpp 50% duty cycle square wave.

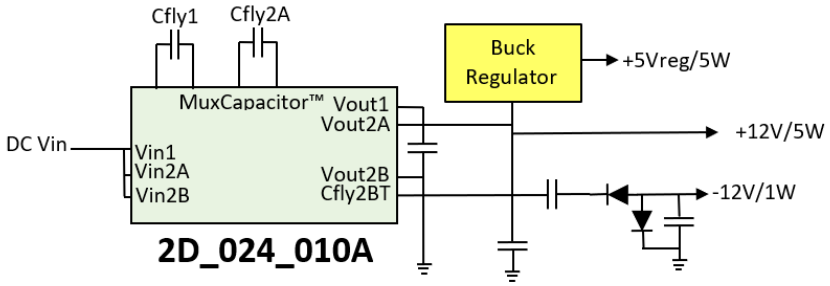

Figure 5. Generating negative and regulated voltage with the MxC200 family

Stage 2A is used to output +12V and as a source for a buck converter to also generate a regulated 5V. Either a linear LDO or switching buck regulator could be used. Make sure there is sufficient headroom for the regulator and output voltage.

Operation of the MxC200 MuxCapacitor charge pump cell:

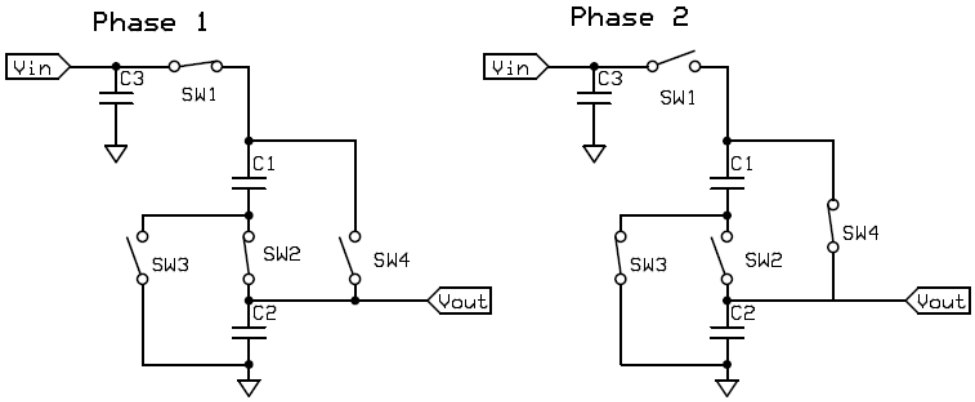

Figure 6. Illustration of charge pump operation.

Evaluating the voltage *reduction* operation for a MuxCapacitor (MuxCap) stage during a switching cycle is straight forward. On the first half cycle, Phase1 in figure 6, the flying cap C1 and output cap C2 are in series, so each holds a voltage charge of ½ x Vin, then in the second half cycle, phase 2, the C1 flying capacitor is placed in parallel with the output capacitor C2, so the voltage across these capacitors are ½ the input voltage. For a voltage *multiplier* the opposite is true; using Figure 6 again, but starting now with phase 2 as an example, the input voltage is now at Vout and charges both the C2 input and C1 flying capacitors in parallel. Then in phase 1 it connects them in series to charge the C3 output capacitor to the input voltage x two. During half of each cycle the output cap supplies the output current alone and the other half cycle both output and flying cap (or flying cap in series with the input cap in boost mode) supply the current in parallel. Generally, a larger flying cap and output cap can deliver more current during a switching cycle as well as reducing the amount of ripple voltage. The amount of sag in the output voltage for a given current load depends mostly on the size of the output capacitor; a larger capacitor will not sag as much during the time the flying capacitor is not in parallel with it. The efficiency of a MuxCap stage is higher when both capacitors are larger when driving larger loads. Eventually a value is reached where the increase in efficiency from adding additional capacitance does not significantly improve the performance. So, the improvement in efficiency needs to be weighed against the added cost for more or larger capacitors. But this also means the values of the capacitors can be optimized for the output current requirements of the application to get the best cost/performance benefit. Therefore, the capacitor values can be selected to get the needed performance for the application without having to pay for a larger capacitor than is needed. A larger output capacitor will reduce ripple, but not necessarily improve efficiency significantly.

Generally, using the same value flying cap and output cap is recommended. Using the same values for the flying and output capacitors may improve efficiency slightly over using different values, but it depends on the requirements of the application. Using the same values for both helps reduce the number of component values in the BOM which can potentially reduce the component costs.

Using MLCC capacitors with the MxC200 family:

To get better performance (efficiency) from a MuxCap stage, caps with lower ESL (effective series inductance) and ESR (effective series resistance) ratings should be used. Multi-Layer Ceramic Capacitors (MLCCs) have these characteristics but are recommended for a number of reasons. MLCCs generally have the lowest ESR and ESL than other capacitor types. They are also usually less expensive than other capacitor technologies, but some care in selection is important. DC voltage derating of MLCC capacitors as well as the rms current rating should be considered when selecting the capacitors. DC voltage derating is a little known, but critical parameter in MLCC type 2 capacitors. The smaller the case size and higher the rated capacitance or higher the rated voltage, the lower the effective capacitance will tend to be with an applied DC bias voltage. This is very pronounced in 0805 (and smaller) case size higher capacitance MLCCs. At lower output currents, this may not be a significant factor, but at higher currents this may reduce efficiency. The over current protection monitors the ripple voltage, so a lower effective capacitance will exhibit more ripple as the load current increases. The best cost/performance has been observed by using two 10uF, 50V 1210 MLCCs in parallel when using the MxC200 family of products. This value capacitor is commonly used in many applications, so the relative cost is lower than for other values that are less popular. Using parallel capacitors, when higher loads are being supported, is generally more cost effective than using capacitors larger than 10uF. If the target application is for a relatively low power design, smaller value caps can be used. Pick your caps carefully since capacitors with different temperature characteristics have different DC derating curves. This can also apply to different manufacturers.

The highest internal voltage is ½ Vin for a given stage, so with a 48V input to Vin1, the maximum the flying and output cap voltage will see is 24V. For a typical 10u/50V 1210 MLCC, the effective capacitance will be ~4.3uF for the first stage. Note this a quite a bit lower than the rated capacitance, but this is better than what would be the case for lower voltage, relatively high capacitance capacitors. For instance, a 22uF, 35V 1206 MLCC capacitor with an applied voltage of 25VDC can have an effective capacitance of 2.2uF; much higher percentage of loss and even less capacitance than the 10uF/50V 1210 MLCC under the same conditions.

The effect of switching frequency on performance:

In the charge pump cell used in the MxC200, in voltage reduction modes the flying cap is connected in series with the output capacitor during the charging cycle and connected in parallel with the output capacitor during the discharge cycle. The flying cap value (along with the parallel output capacitor) and load current determine the amount of ripple voltage that will appear at the output of each stage, and

therefore the maximum power a MuxCap stage can deliver in a switching cycle. If the switching frequency is increased, the ripple voltage is reduced because there is less time for the capacitors to discharge before the next charging cycle begins. Neglecting the switching losses, this means that the efficiency of a MuxCap stage can be higher at higher switching frequencies due to the lower ripple voltage (higher average voltage). Conversely, a higher switching frequency causes higher switching losses (and gate drive losses), so this is a tradeoff that needs to be evaluated carefully depending on the application.

For MxC200 the sweet spot for switching frequency at mid/high loads is between 100kHz and 200kHz. At light loads, a low switching frequency yields better efficiency. Therefore, if a MxC200 is feeding a Buck converter and the Buck switching frequency slows down at light loads, it is beneficial to synchronize MxC200 to the Buck switching frequency to lower the MxC200 switching frequency, and hence improve the light-load efficiency. This is done by using the external clock enable and supplying the external clock pin with the clock from the switching regulator. This has been shown to improve efficiency at light loads.

Parallel Operation

Another interesting feature of the MxC200 family is that they can also be connected in parallel. If more power is needed than can be supplied by a single device, they can easily be connected in parallel. Each device self regulates such that they will share the loads equally. Special circuitry is not required to do this. The inputs and outputs of each section can be connected to the like signal on another device to increase the power that can be supplied. This means the DC Vin and Vout of each device can be connected to the like pin(s) on another device. Other pins, such as the Cflys and other dynamic or internal pins, should be not be connected together. The reason these pins cannot be connected is that the clocking for the flying capacitors and bridge drivers are not coming from a common timing source and would interfere with each other if those signals were connected from different devices. Multiple MxC200 devices have been connected in this way to provide up to a kilowatt or more of power.

Layout Considerations:

Keeping MxC200 cool is essential for maintaining high efficiency and being able to deliver reliable maximum power. The switch impedances go up as a function of the current due to heat dissipated in the FETs. If the heat dissipation from the package to the PCB and the environment is not effective, efficiency drops as the switch resistance increases (FET Rdson has a positive temperature coefficient) and the maximum deliverable output power is lowered. The MxC200 family is mainly cooled through the center ground pad. Therefore, it is strongly recommended to use multiple “vias” to effectively connect this pad to the bottom exposed ground plane and the other layers of PCB. Satisfactory results are obtained with a 4-layer board with two layers of ground plane (top and bottom) and 9 vias connecting the center pad to the ground planes. Nine 0.031-inch vias fit under the center pad, and it is recommended to use filled vias. Wide paths should be used as much as possible for connection to the inputs, outputs, and flying caps. Also, filled vias are recommended for these high current paths. Connect all ground pins to the center ground pad.

The above recommendation is based on a 1oz copper PCB but using 2oz copper improves the performance of the device at higher output powers.

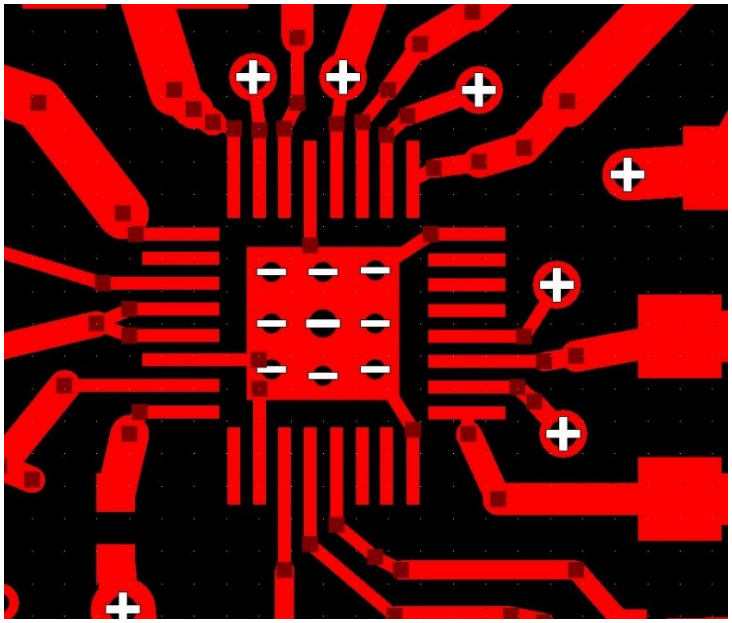

Figure 7. An example of the top layer of the PCB showing the required vias on the central pad of MxC200. The vias connect the center pad to the ground plane in other layers of the PCB and provide a thermal path for extracting heat from the device.

In Conclusion

The MxC200 family are very flexible devices that can help achieve the highest efficiency in a power supply design. They complement the use of inexpensive, low input voltage regulators in point of load designs. They can be used to decrease or increase the voltages available from a single power source simply and efficiently at a very reasonable cost. Inductors are not required when using the MxC200 which also helps reduce cost. It is highly effective at converting a voltage to higher or lower levels and can even be used to generate a negative supply if it is required.