

### HS100 MuxCapacitor® Plus Forward Converter Chip Set

The Helix Semiconductors HS100 Mux-Capacitor Plus Forward Converter two-chip set solution offers the highest energy efficiency for a 110VAC/10W or 220VAC/5W AC-DC isolated power supply. A multi-gain MuxCapacitor delivers the optimum voltage to a forward converter. The forward converter employs an advanced pulse skipping algorithm to maximize no-load and standby operation power efficiency.

The HS100 two chip set includes reset, internal references and regulation & gain control logic. The chip set's high efficiency reduces thermal loading for lower packaging costs. Other output voltages are available with a simple gain trim.

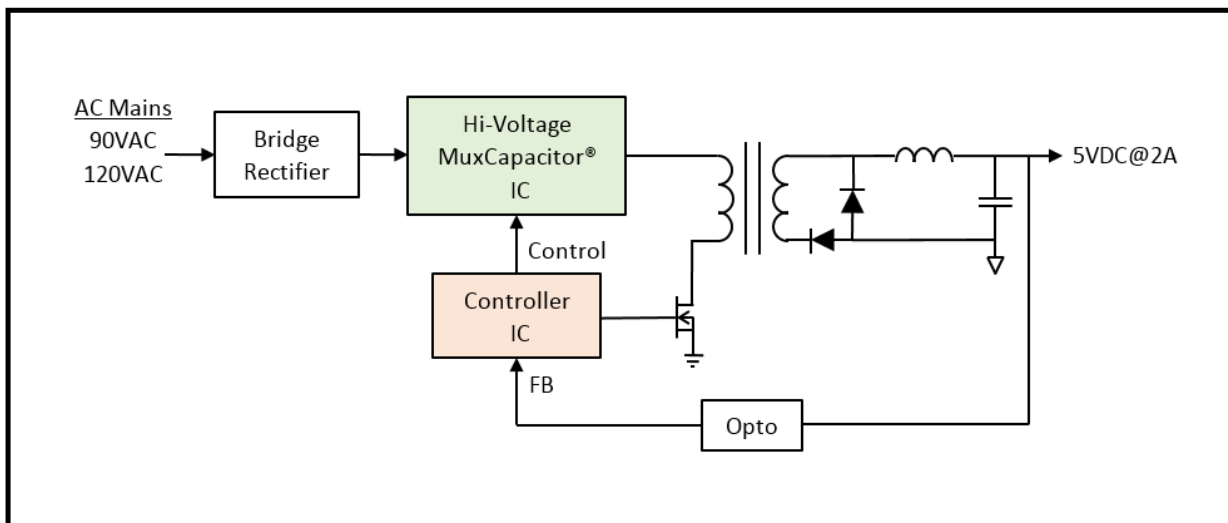
### Features

- 85-264VAC Input Voltage
- High Voltage MuxCapacitor
- Soft-Start
- 5V, 2A Output Voltage @ 120VAC
- 5V, 1A Output Voltage @ 240VAC
- ±5% Output Voltage Regulation
- > 95% Efficiency @ 2A
- > 92% Efficiency @ 200mA
- 10mW No-Load Power Consumption

### Applications

- Smart Outlets
- IoT and IIoT Gateways
- Remote Sensors
- Smoke and CO Detectors

### HS100 Block Diagram





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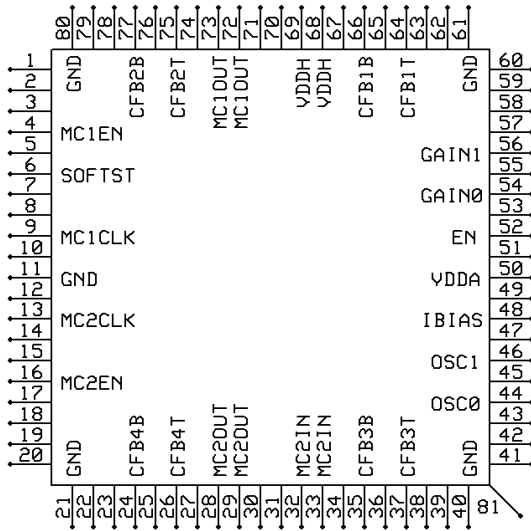
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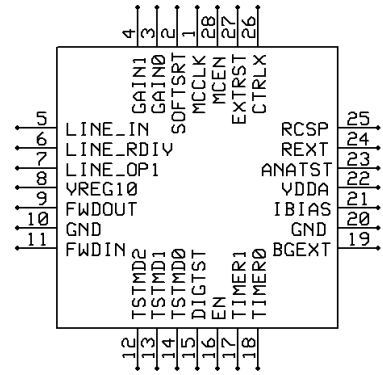
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### 1 Pin Configuration and Description

Figure 1: Pin Configuration



HS100 MuxCapacitor IC – QFN80



HS100 Control IC – PLCC28



The HS100 chip set is provided in prototype packaging for test development purposes ONLY. Special handling precautions are required due to the presence of high voltage.

Table 1: HS100 MuxCapacitor IC Pin Assignments

Pin No.	Name	Description
4	MC1EN	MuxCapacitor 1 Enable: Input Pin 0 = Disable, 1 = Enable Internal Pull-Down
6	SOFTST	Soft-Start Timer: Input Pin 0 = Disable, 1 = Enable Internal Pull-Down



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9	MC1CLK		MuxCapacitor 1 Clock: Input Pin																				
11	GND		Low Voltage Ground																				
13	MC2CLK		MuxCapacitor 2 Clock: Input pin																				
16	MC2EN		MuxCapacitor 2 Enable: Input Pin 0 = Disable, 1 = Enable Internal Pull-Down																				
21, 40, 61, 80	GND		High Voltage Ground																				
24	CFB4B		External Flying Capacitor 4 (-)																				
26	CFB4T		External Flying Capacitor 4 (+)																				
28, 29	MC2OUT		MuxCapacitor 2: Analog Output Pin																				
32, 33	MC2IN		External MuxCapacitor 2: Analog Input Pin																				
35	CFB3B		External Flying Capacitor 3 (-)																				
37	CFB3T		External Flying Capacitor 3 (+)																				
44 46	OSCO OSC1		Oscillator Frequency Control: Input Pins <table border="1"> <thead> <tr> <th>OSC1</th> <th>OSCO</th> <th>Freq Out - MHz</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1.6 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>0.8 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>0.4 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>Disabled</td> </tr> </tbody> </table> Internal Pull-Downs	OSC1	OSCO	Freq Out - MHz	0	0	1.6 MHz	0	1	0.8 MHz	1	0	0.4 MHz	1	1	Disabled					
OSC1	OSCO	Freq Out - MHz																					
0	0	1.6 MHz																					
0	1	0.8 MHz																					
1	0	0.4 MHz																					
1	1	Disabled																					
48	IBIAS		1 $\mu$ A Bias Current Reference: Analog Input Pin																				
50	VDDA		+5V Supply Voltage: Analog Input Pin																				
52	EN		Device Enable: Input Pin 0 = Disable, 1 = Enable Internal Pull-Down																				
54 56	GAIN0 GAIN1		MuxCapacitor Gain Control: Input Pins <table border="1"> <thead> <tr> <th>GAIN1</th> <th>GAIN0</th> <th>MX1 Gain</th> <th>MX0 Gain</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>2/3</td> <td>2/3</td> </tr> <tr> <td>1</td> <td>0</td> <td>1/2</td> <td>1/2</td> </tr> <tr> <td>1</td> <td>1</td> <td>2/3</td> <td>1/2</td> </tr> </tbody> </table> Internal Pull-Downs	GAIN1	GAIN0	MX1 Gain	MX0 Gain	0	0	1	1	0	1	2/3	2/3	1	0	1/2	1/2	1	1	2/3	1/2
GAIN1	GAIN0	MX1 Gain	MX0 Gain																				
0	0	1	1																				
0	1	2/3	2/3																				
1	0	1/2	1/2																				
1	1	2/3	1/2																				
64	CFB1T		External Flying Capacitor 1 (+)																				
66	CFB1B		External Flying Capacitor 1 (-)																				
68, 69	VDDH		MuxCapacitor 1: Analog Input Pin																				
72, 73	MC1OUT		MuxCapacitor 1: Analog Output Pin																				
75	CFB2T		External Flying Capacitor 2 (+)																				




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77	CFB2B 	External Flying Capacitor 2 (-)
81	TPAD	Thermal Pad: No Connection
1,2,3,5, 7,8,10,12,14,15, 17,14,15,17,18,19,20,22, 23,25,27,30,31,34,36,38, 39,41,42,43,45,47,49,51, 53,55,57,58,59,60,62,63, 65,67,70,71,74,76,78.79		Unused, Do Not Connect

**Table 2: HS100 Control IC Pin Assignments**

Pin No.	Name	Description																																				
1	MCCLK	MuxCapacitor Clock: Output Pin																																				
2	SOFSTRT	Soft Start Timer: Output Pin																																				
3	GAIN0	MuxCapacitor Gain Control: Output Pins																																				
4	GAIN1																																					
5	LINE_IN 	Rectified Line Voltage: High Voltage Analog Input Pin																																				
6	LINE_RDIV	Line Voltage Resistor Divider: Analog Input Pin																																				
7	LINE_OP1	Source Follower pin from LINE_RDIV Add external 0.1 $\mu$ F, 50V capacitor																																				
8	VERG10	+10V Regulator: Analog Output Pin Add external 10 $\mu$ F, 16V capacitor																																				
9	FWDOUT	Forward Converter FET Driver: Output Pin																																				
10	GND	Low Voltage Ground																																				
11	FWDIN	Forward Converter Opto Feedback: Analog Input Pin																																				
12	TSTMD2	Test Mode Control: Input Pins <table border="1" data-bbox="574 1367 1409 1732"> <thead> <tr> <th>TSTMD2</th> <th>TSTMD1</th> <th>TSTMD0</th> <th>Test Mode Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>DIGTST: OC Detect</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>DIGTST: FWD Clamp</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>DIGTST: FWD Softstart OK</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>DIGTST: 100kHz Ocsillator</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Reset OC Detect</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Disable FWD PID</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>ANATST: Bandgap Voltage</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Logic Test Mode</td> </tr> </tbody> </table> Internal Pull-Downs	TSTMD2	TSTMD1	TSTMD0	Test Mode Operation	0	0	0	DIGTST: OC Detect	0	0	1	DIGTST: FWD Clamp	0	1	0	DIGTST: FWD Softstart OK	0	1	1	DIGTST: 100kHz Ocsillator	1	0	0	Reset OC Detect	1	0	1	Disable FWD PID	1	1	0	ANATST: Bandgap Voltage	1	1	1	Logic Test Mode
TSTMD2	TSTMD1		TSTMD0	Test Mode Operation																																		
0	0		0	DIGTST: OC Detect																																		
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0	1		1	DIGTST: 100kHz Ocsillator																																		
1	0		0	Reset OC Detect																																		
1	0		1	Disable FWD PID																																		
1	1		0	ANATST: Bandgap Voltage																																		
1	1	1	Logic Test Mode																																			
13	TSTMD1																																					
14	TSTMD0																																					
15	DIGTST	Digital Test Mux: Output Pin																																				
16	EN	Device Enable: Input Pin																																				



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		0 = Disable, 1 = Enable Internal Pull-Down															
17 18	TIMER1 TIMERO	Soft Start Timer Control: Input Pins <table border="1"> <thead> <tr> <th>TIMER1</th> <th>TIMERO</th> <th>Soft Start Delay</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>10 msec</td> </tr> <tr> <td>0</td> <td>1</td> <td>30 msec</td> </tr> <tr> <td>1</td> <td>0</td> <td>20 msec</td> </tr> <tr> <td>1</td> <td>1</td> <td>40 msec</td> </tr> </tbody> </table> Internal Pull-Downs	TIMER1	TIMERO	Soft Start Delay	0	0	10 msec	0	1	30 msec	1	0	20 msec	1	1	40 msec
TIMER1	TIMERO	Soft Start Delay															
0	0	10 msec															
0	1	30 msec															
1	0	20 msec															
1	1	40 msec															
19	BGEXT	Optional External 1.25V Bandgap: Analog Input Pin Set CTRLX = 1 for use with external bandgap.															
20	GND	Low Voltage Ground															
21	IBIAS	Bias Current Reference: Analog Output Pin															
22	VDDA	+5V Regulator: Analog Output Pin Add external 10 $\mu$ F, 16V capacitor															
23	ANATST	Analog Test Mux: Output Pin															
24	REXT	External Bias Resistor: Analog Input Pin Add external 499K 1% resistor from REXT pin to GND															
25	RCSP	Forward Converter Current Sense: Analog Input Pin Add external 0.5 $\Omega$ 1% current sense resistor to GND.															
26	CTRLX	Control/Test Mode: Input Pin 0 = Disable, 1 = Enable Control Mode and Test Modes Internal Pull-Down															
27	EXTRST	External Reset: Input Pin 0 = Disable, 1 = Enable Internal Pull-Down															
28	MCEN	MuxCapacitor Enable: Output Pin															





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## 2 Absolute Maximum Ratings

The HS100 chip-set can be exposed to the following extremes without permanent damage to device operation. Performance is not guaranteed at these extremes.

**Table 3: Absolute Maximum Ratings**

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$V_{HVIO}$	Voltage at all High-Voltage Analog I/O	-0.3		350	V	At pins VDDH, MC2IN, LINE_IN
$V_{MVIO}$	Voltage at all Mid-Voltage Analog I/O	-0.3		40	V	At pins LINE_RDIV, LINE_0P1
$V_{LVIO}$	Voltage at all Low-Voltage I/O	-0.3		6.0	V	
$V_{HBM}$	HBM ESD Voltage			2	KV	Human Body Model
$V_{CDM}$	CDM ESD Voltage			500	V	Charge Device Model
$V_{MM}$	MM ESD Voltage			200	V	Machine Model
$V_{LU}$	Latchup Test Limits	-100		100	mA	
$T_{store}$	Storage Temperature Range	-40		125	°C	
$T_j$	Junction Temperature Range	-40		125	°C	



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### 3 Recommended Operating Conditions

The HS100 chip-set is designed to operate within the design limits specified in the Parametric Specifications when the conditions of the following table are not exceeded.

**Table 4: Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$V_{HVIO}$	Voltage at all High-Voltage Analog I/O	127	170	340	V	At pins VDDH, MC2IN, LINE_IN
$V_{MVIO}$	Voltage at all Mid-Voltage Analog I/O	12.7	17.0	34.0	V	At pins LINE_RDIV, LINE_OP1
$V_{LVIO}$	Voltage at all Low-Voltage Analog I/O	4.5	5.0	5.5	V	
$T_a$	Ambient Temperature Range	-40		85	°C	
$T_j$	Junction Temperature Range	-40		125	°C	



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### 4 Parametric Specifications

The electrical characteristics of the HS100 Chip-Set are tested according to the following criteria noted in the Test column of each table:

- T : Directly or indirectly tested at 100% for production or prototype samples
- Q : Tested for qualification and bench evaluation
- D : Guaranteed by Design

All specifications apply only to the HS100 Control IC unless otherwise noted.

**Table 5: Line-Side Bandgap Voltage Reference**

Symbol	Parameter	Conditions	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>LINE0P1</sub>	Supply Voltage	At LINE_0P1	D	12.7		34.0	V
I <sub>LINE0P1</sub>	Supply Current	At LINE_0P1; en=1	D		8.3		μA
V <sub>BG</sub>	Output Voltage	At ANATST; No trim	T	1.158	1.219	1.28	V
V <sub>TOL</sub>	Output Voltage Tolerance	At ANATST; No trim	T			±5	%
T <sub>c</sub>	Temp. coefficient	At ANATST	Q			300	ppm/°C
PSR	Power Supply Rejection	At ANATST; f=10KHz & 100KHz	Q	70			dB <sub>20</sub>
PSR <sub>DC</sub>	DC supply rejection	At DC; f=0.001Hz	Q	90			dB <sub>20</sub>
V <sub>N</sub>	Output Noise	Integrated Noise; 10Hz ≤ f ≤ 10KHz	D			1000	μVrms
I <sub>BIAS</sub>	Output Current	At IBIAS; T=25°C; R <sub>EXT</sub> =500KΩ 1%	D	0.94	1.0	1.06	μA
C <sub>L</sub>	Output Load Capacitance	At VBG	D			2	pF
t <sub>RAMP</sub>	Supply Ramp Time	At LINE_0P1	D	0.1		100	mS
t <sub>s</sub>	Startup time	At VBG; For 100μS ramp at LINE_0P1	D			2000	μS
I <sub>LKG</sub>	Disabled Leakage Current	en=0	D			10	nA

- Notes:
1. Min and Max values are valid over Operating Conditions, unless otherwise stated.
  2. Typ values are valid at typical Operating Conditions and typical process Parameters.



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**Table 6: 5.0V Linear Voltage Regulator**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>REF</sub>	Reference Input Voltage	Bandgap voltage at V <sub>BG</sub>	D		1.219		V
V <sub>OUT</sub>	Output Voltage	At VDDA; 100μA ≤ I <sub>LOAD</sub> ≤ 10mA	T	4.5	5.0	5.5	V
VR	Line Regulation	At VDDA; I <sub>LOAD</sub> = 2mA;	T			100	m%
LR	Load Regulation	At VDDA; 0 ≤ I <sub>LOAD</sub> ≤ 10mA	T			100	m%
A <sub>OL</sub>	Open Loop Gain	In-Circuit; I <sub>LOAD</sub> = 2mA C <sub>LOAD</sub> = 11μF,	D	90			dB
		I <sub>LOAD</sub> = 1μA	D	80			
φ <sub>M</sub>	Phase Margin	In-Circuit; I <sub>LOAD</sub> = 2mA C <sub>LOAD</sub> = 11μF	D	70			Deg.
		I <sub>LOAD</sub> = 1μA	D	65			
PSRR	Power Supply Rejection Ratio	f=10KHz; C <sub>L</sub> =11μF; I <sub>LOAD</sub> = 2mA	Q	40			dB
		f=dc; C <sub>L</sub> =11μF; I <sub>LOAD</sub> = 2mA	Q	60			dB
V <sub>OS</sub>	Input-Referred Offset	6σ Mismatch; I <sub>LOAD</sub> = 2mA	D			15	mV
I <sub>SUP</sub>	Power Supply Current	en=1; No Load;	D			1	μA
I <sub>LKG</sub>	Off-State Leakage Current	en=0; No Load	D			10	nA

Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
2. Typ values are valid at typical Operating Conditions and typical process Parameters.



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**Table 7: Power-On-Reset**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>SUP</sub>	Supply Voltage	At V <sub>DDA</sub>	D	4.5	5.0	5.5	V
V <sub>POR</sub>	POR Threshold		Q	2.8	3.0	3.2	V
V <sub>HYS</sub>	Input Voltage Hysteresis		Q	200	300	450	mV
I <sub>SUP</sub>	Enabled Drain Current	For information only	D		3.1		μA

Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
 2. Typ values are valid at typical Operating Conditions and typical process Parameters.

**Table 8: Hysteresis Comparators (Country Selector)**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>ICM</sub>	Input Common-Mode Voltage Range		D	0.7	1.25	2	V
A <sub>v</sub>	Voltage Gain	L>H at OUT; V <sub>ICM</sub> =1.25V; Hyst OFF	D	1.0			KV/V
		H>L at OUT; V <sub>ICM</sub> =0.9V; Hyst OFF	D	1.0			
V <sub>HYST</sub>	Input Hysteresis	hyst<1:0>=0	Q		0		mV
		hyst<1:0>=1	Q		10		
		hyst<1:0>=2	Q		20		
		hyst<1:0>=3	Q		30		
t <sub>PD_LH</sub>	Comparator Prop. Delay – Low to High	3mV Overdrive	D			20	μS
t <sub>PD_HL</sub>	Comparator Prop. Delay – High to Low	3mV Overdrive	D			20	μS
t <sub>RISE</sub>	Output Rise Time	3mV Overdrive	D			10	nS
t <sub>FALL</sub>	Output Fall Time	3mV Overdrive	D			10	nS
I <sub>VDDA</sub>	Power Supply Current	en=1; V <sub>DDA</sub> = 5.0V	D		1.8		μA
I <sub>LKG</sub>	Off-State Leakage Current	en=0; V <sub>DDA</sub> = 5.0V	D			10	nA

Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
 2. Typ values are valid at typical Operating Conditions and typical process Parameters.



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**Table 9: MuxCapacitor® Voltage Divider (MuxCapacitor IC only)**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>IN</sub>	Input Voltage	At VDDH / MCIN2 pins	D	90	170	340	V
P <sub>EFF</sub>	Power Efficiency	At I <sub>MCOUTx</sub> =50mA	T	95			%
V <sub>OLT</sub>	MuxCapacitor Output Voltage	I <sub>MCOUT</sub> =50mA	T	90	110	130	V
F <sub>sw</sub>	Switching Frequency		D		1		KHz
T <sub>ST</sub>	SoftStart Timer Period	Programmable via the Low-Voltage IC	D		10		mS
C <sub>FLYBK</sub>	Flyback Capacitance		D		3.3		μF
C <sub>HOLD</sub>	Hold Capacitance		D		7.5		μF
R <sub>OLT</sub>	Output Resistance		D		30		Ω
I <sub>MCOUT</sub>	Output Load Current Range	At MCOUTx	T	0		50	mA
I <sub>SLP</sub>	Enabled Current Drain	Single stage (static+fcV)	D			120	μA
I <sub>LKG</sub>	Disabled Current Drain		D			0.2	μA

Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
 2. Typ values are valid at typical Operating Conditions and typical process Parameters.

**Table 10: Low-Frequency RC Oscillator**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
f <sub>OSC</sub>	Oscillator Frequency	At DIGTST	T	70	100	130	KHz
f <sub>ERR</sub>	Frequency Accuracy	No Trim	T	-30		+30	%
t <sub>CCJ</sub>	Cycle-to-Cycle Jitter		Q		25		nS
t <sub>START</sub>	Startup Time		D		200		μS
DC	Output Duty Cycle		Q	45	50	55	%
I <sub>SUP</sub>	Drain Current	For information only	D			0.5	μA
I <sub>LKG</sub>	Off-State Leakage Current	En=0	D			10	nA

Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
 2. Typ values are valid at typical Operating Conditions and typical process Parameters.



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**Table 11: 3.2MHz Oscillator (MuxCapacitor IC only)**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>SUP</sub>	Supply Voltage	At VDDA	D	4.5	5.0	5.5	V
f <sub>OSC</sub>	Oscillator Output Frequency	OSC<1:0>=0x0	T	1.12	1.6	2.08	MHz
		OSC<1:0>=0x1		0.56	0.8	1.04	
		OSC<1:0>=0x2		0.28	0.4	0.52	
		OSC<1:0>=0x3		-	-	-	
f <sub>ERR</sub>	Frequency Accuracy	No Trim	T	-30		30	%
DC	Output Duty Cycle		Q	45	50	50	%
t <sub>START</sub>	Startup Time		D		10		μS
I <sub>SUP</sub>	Drain Current	For information only	D			20	μA
I <sub>LKG</sub>	Off-State Leakage Current		D			10	nA

- Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
 2. Typ values are valid at typical Operating Conditions and typical process Parameters.

**Table 12: Sawtooth Generator**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>SUP</sub>	Supply Voltage	At VDDA	D	4.5	5.0	5.5	V
f <sub>CLK</sub>	Clock Frequency		D		100		KHz
V <sub>ICM</sub>	Common-Mode Input Voltage		D	0	1.25	2	V
V <sub>OUT</sub>	Output Voltage (Pk-Pk)		D	1.9	2.7	3.5	V <sub>PP</sub>
I <sub>SUP</sub>	Drain Current	For information only	D			20	μA
I <sub>LKG</sub>	Off-State Leakage Current	En=0	D			10	nA

- Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
 2. Typ values are valid at typical Operating Conditions and typical process Parameters.



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**Table 13: Forward PID Control Loop**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>IN</sub>	Input Voltage Range	Scaled Input Voltage	D	0	1.25	5	V
REG <sub>PID</sub>	Output Regulation	At Forward Converter output; $0 \leq I_{LOAD} \leq 2A$	Q	-5		+5	%
LBW <sub>PID</sub>	Loop Bandwidth		Q			10	KHz
PM <sub>PID</sub>	Phase Margin		D		70		Deg
f <sub>Z1</sub>	First Zero Frequency	Filtered PID	D		1.7		KHz
f <sub>Z2</sub>	Second Zero Freq.	Differentiator Response	D		3.4		KHz
f <sub>P1</sub>	First Pole Frequency	Integrator Response	D		3.4		KHz
f <sub>P2</sub>	Second Pole Freq.	Proportional Pole	D		56		KHz
f <sub>PWM</sub>	PWM Switching Freq.		D		100		KHz
DC <sub>MAX</sub>	Max Clamped Duty Cycle		Q	--	65	--	%
OCP	Over Current ProtectionThreshold		T	--	2.5	--	A
T <sub>START</sub>	Startup Time	Due to soft start	Q	--	1	1.6	ms
I <sub>VDDA</sub>	Current Drain		D	--	--	20	μA
I <sub>LKG</sub>	Off-State Leakage Current		D	--	--	10	nA

Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
 2. Typ values are valid at typical Operating Conditions and typical process Parameters.





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**Table 14: CMOS Digital Inputs (TTL)**

Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>IL</sub>	Input Low Voltage	4.5V ≤ V <sub>DDA</sub> ≤ 5.5V	D	-0.3		0.8	V
V <sub>IH</sub>	Input High Voltage	4.5V ≤ V <sub>DDA</sub> ≤ 5.5V	D	2.0		V <sub>DDIO</sub> + 0.3V	V
I <sub>LEAK</sub>	Input Leakage Current	No Pull Up/Down		-10		10	μA
I <sub>PD</sub>	Input with Pull Down	At CTRLX, TSTMD<2:0> EN, TIMER1, TIMER0		3	15	40	μA

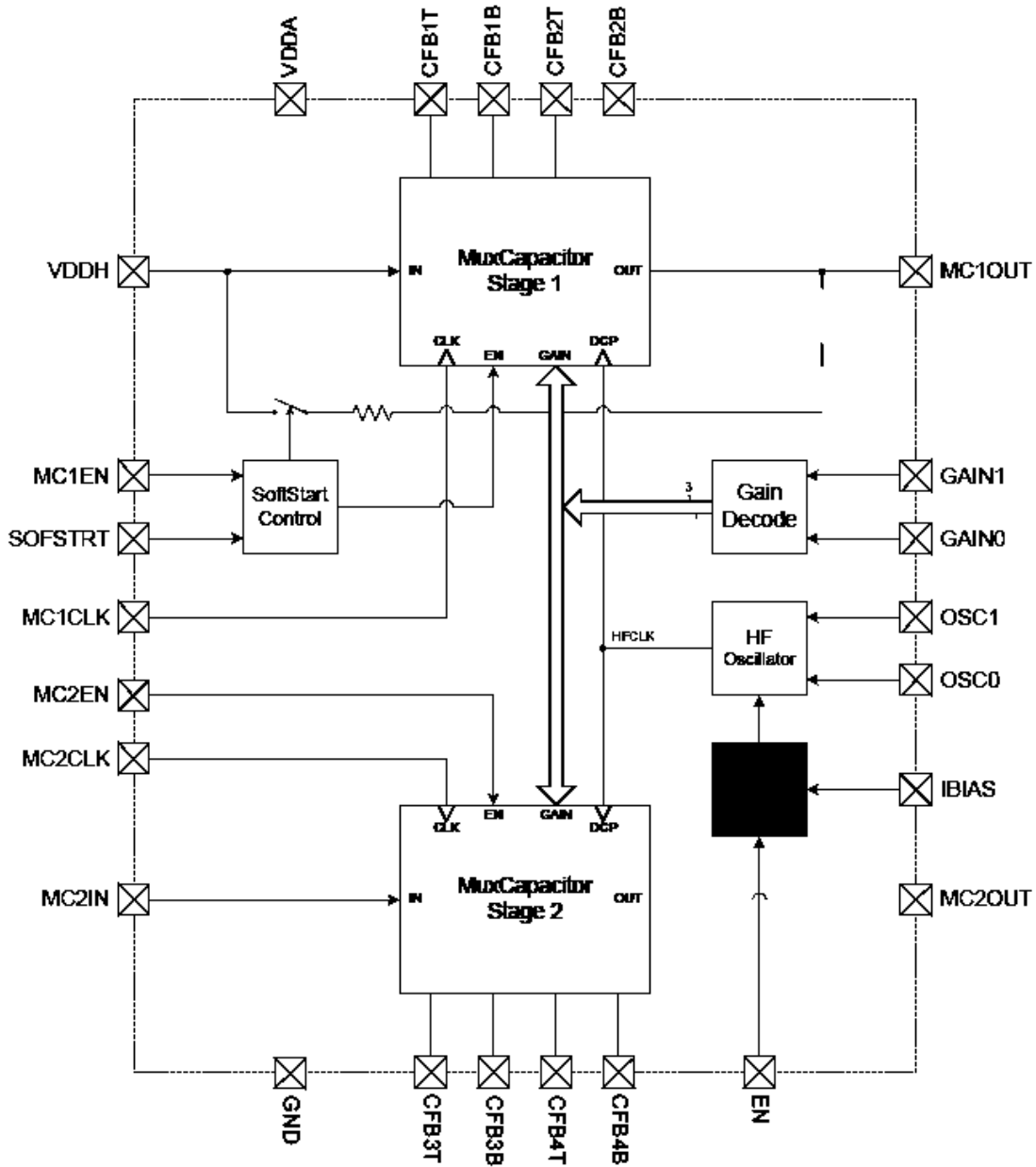
Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
2. Typ values are valid at typical Operating Conditions and typical process Parameters.

**Table 15: CMOS Digital Outputs (TTL)**

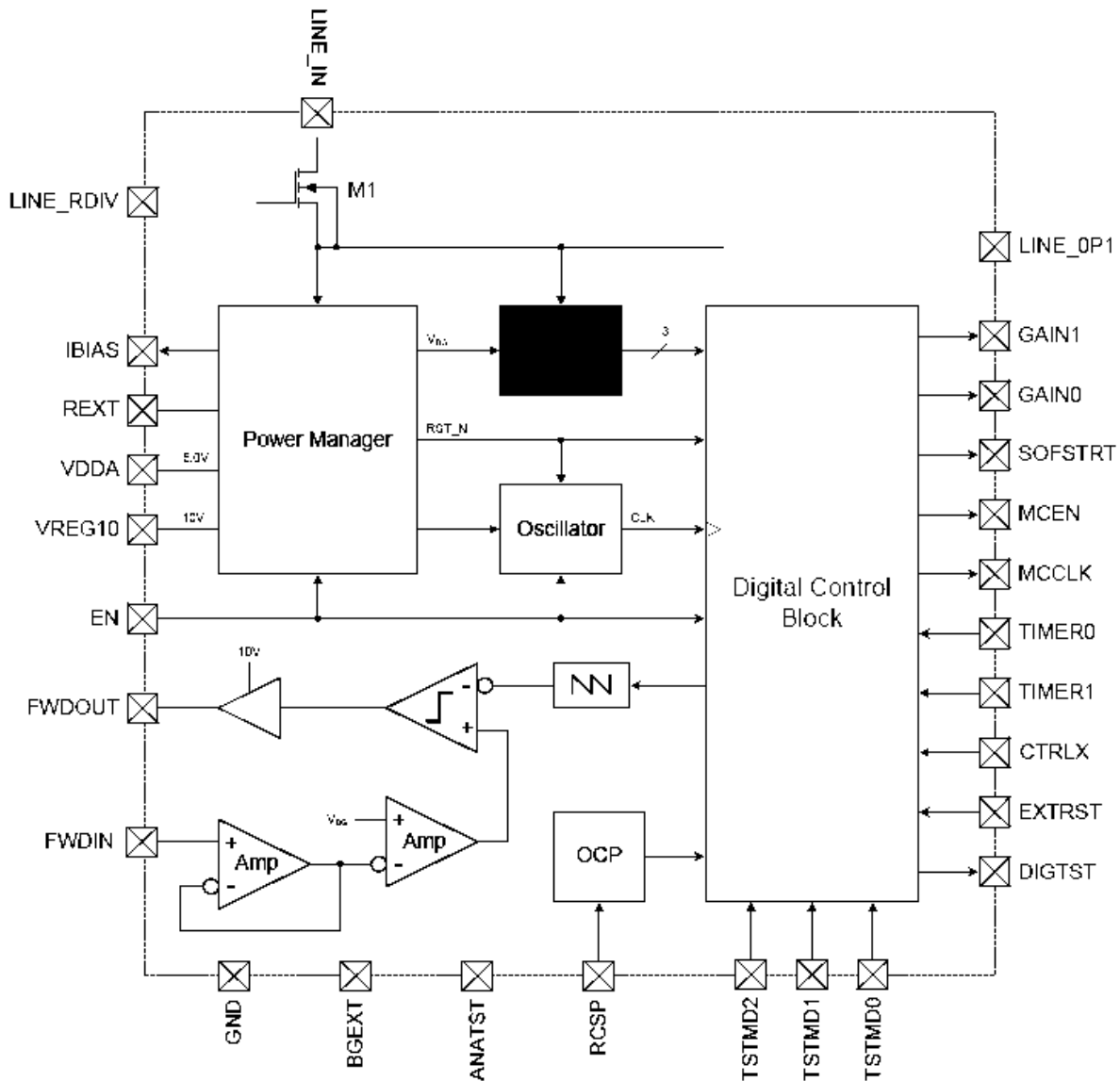
Symbol	Parameter	Condition	Test	Min <sup>1</sup>	Typ <sup>2</sup>	Max <sup>1</sup>	Unit
V <sub>OL</sub>	Output Low Voltage	4.5V ≤ V <sub>DDA</sub> ≤ 5.5V	D			0.4	V
V <sub>OH</sub>	Output High Voltage	4.5V ≤ V <sub>DDA</sub> ≤ 5.5V	D	2.4			V
I <sub>OH</sub>	Output Current	4.5V ≤ V <sub>DDA</sub> ≤ 5.5V				1	mA

Notes: 1. Min and Max values are valid over Operating Conditions, unless otherwise stated.  
2. Typ values are valid at typical Operating Conditions and typical process Parameters.

Figure 2: HS100 MuxCapacitor IC Block Diagram



**Figure 3: HS100 Control IC Block Diagram**





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## 5 Functional Description

The Helix Semiconductors HS100 chip-set is comprised of two ICs: MuxCapacitor IC and Control IC. The HS100 chip-set reduces the rectified AC line voltages of 90V – 240V to 5.0VDC with an output current of up to 2.0A for AC line voltages 90- 120VAC or up to 1A for 220-240VAC.

### 5.1 HS100 MuxCapacitor IC

The HS100 MuxCapacitor IC contains all of the high-voltage circuitry required for reducing the rectified AC Mains voltage to an optimal primary-side voltage for a forward converter isolation transformer. Startup and control of the MuxCapacitor IC is provided by the companion HS100 Control IC.

The block diagram of the HS100 MuxCapacitor IC illustrates the two MuxCapacitor voltage-divider stages and the required support circuitry. Each MuxCapacitor stage can be independently configured for either parallel or series connectivity as required by the application. For increased current capability, the two MuxCapacitor stages can be externally connected in parallel for 2X the current of a single MuxCapacitor stage.

For greater voltage division, the MuxCapacitors can be externally cascaded to provide a reduced voltage at the IC's output. For all cascaded (or series connected) applications the first MuxCapacitor stage must be connected to the highest input voltage at the VDDH pin. The MuxCapacitor output at MC1OUT is then connected to the second MuxCapacitor input at MC2IN.

A Soft-Start current limiting switch is included to limit the inrush current from the VDDH input. Additional resistance in series with the switch limits the current to protect the MuxCapacitor power transfer switches until the external hold capacitor at MC1OUT is fully charged. The time period for the Soft-Start feature is controlled by the Control IC and output to the MuxCapacitor's SOFSTRT input.

An on-chip oscillator provides a 1.6MHz clock for the Dickson Charge Pump (DCP) voltage boosters. The voltage boosters provide the high side gate signals to the MuxCapacitor stages. The bias current for the Oscillator as well as the MuxCapacitor stages is provided by the IBIAS input.



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### 5.1.1 MuxCapacitor Voltage Divider

The HS100 MuxCapacitor IC voltage dividers reduce the DC voltage present at their input pins to a lower voltage at their respective MCxOUT pins. Each MuxCapacitor stage has a programmable gain of 1.0, 0.66 or 0.5 set by the GAIN1 and GAIN0 input pins. The truth table for the gain selection of the MuxCapacitor stages is shown in the table below.

**Table 16: MuxCapacitor Gain Selection Truth Table**

Input Pin		MuxCapacitor Gain	
GAIN1	GAIN0	Stage 1	Stage 2
0	0	1	1
0	1	0.66	0.66
1	0	0.5	0.5
1	1	0.66	0.5

Each MuxCapacitor stage can deliver up to 50mA of current. The output voltage is dependent on the gain setting and the input voltage. Two external fly-back capacitors and a hold capacitor are required per MuxCapacitor stage. These capacitors are connected to the CFBxT, CFBxB, and MCxOUT pins, respectively. The MuxCapacitor stages are clocked at a rate of up to 1KHz from the MCxCLK input clock pin. The duty cycle of the clock is 50%.

### 5.1.2 Dickson Charge Pumps

The Dickson Charge Pumps (DCP's) are used to provide a boosted voltage for the gates of the NMOS high-voltage switches. The MuxCapacitor has multiple high side switches and each switch has a DCP that is clocked at 1.6 MHz. The DCPs generate a voltage that is 15V greater than the voltage at the MuxCapacitor's input pin. The DCP's clock is provided by the High-Frequency Oscillator.

### 5.1.3 Level Shifters

Each NMOS high-voltage switch has a corresponding level shifter to translate the drive signal from the low-voltage domain to the boosted voltage provided by the DCP's. Each high-voltage switch has an optimally sized level shifter based on its gate drive characteristics.

### 5.1.4 Soft-Start Current Limiter

A Soft-Start current limiting switch is provided for the first MuxCapacitor stage to limit in-rush current at startup. The switch and a series connected resistor are placed in parallel with the primary power



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switches from the input to the output of the MuxCapacitor stage. The current is limited by the resistor when the switch is enabled.

The Soft-Start sequence is initiated and controlled by a programmable timer located in the HS100 Control IC. During the SOFTST timer period all MuxCapacitor power transfer switches are disabled to eliminate any low-resistance paths from input to output. Once the timer completes the cycle, all switches are then enabled for normal operation. The current limiting switch is enable by setting the SOFTST pin high. The MuxCapacitor is enabled by setting the MC1EN pin high. Therefore, during soft start, SOFTST = 1 and MC1EN = 0. For noraml operation, SOFTST = 0 and MC1EN = 1.

### 5.1.5 3.2MHz Oscillator

The 3.2MHz Oscillator provides the high-frequency clock for the HS100 MuxCapacitor IC. It contains a divide-by-two to produce a 1.6MHz, 50% duty cycle clock for the Dickson Charge Pumps for each MuxCapacitor stage. The frequency of the oscillator can be programmed with the OSC1 and OSC0 pins according to the following table.

**Table 17: Oscillator Frequency Control**

Input Pin		Oscillator Frequency
OSC1	OSC0	
0	0	1.6MHz
0	1	0.8MHz
1	0	0.4MHz
1	1	Disabled



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### 5.2 HS100 Control IC

The HS100 Control IC provides all the low-voltage bias and support circuitry required for startup and control of the HS100 MuxCapacitor IC and the external Forward Converter.

The rectified AC-Mains voltage is input at the LINE\_IN pin to provide power to the Control IC. An on-chip source follower M1 reduces the voltage for internal Low Drop-Out (LDO) regulators. An external resistor divider at the LINE\_RDIV pin provides the gate bias for M1 such that the voltage at LINE\_OP1 (M1 drain) is 1/10 of the incoming LINE\_IN voltage. The LINE\_OP1 voltage is used to supply all of the internal circuits on the Control IC.

The LINE\_OP1 voltage is also used to sense the incoming AC-Mains voltage and is input to the Country Selector. The Country Selector determines the proper gain setting for the MuxCapacitor IC by setting the GAIN0 and GAIN1 outputs of the Digital Control Block as a function of the region of operation, i.e. Japan/US or Universal.

The Power Manager provides all the reference voltages and currents for the Control IC. The following circuits reside within the Power Manager: Bandgap Voltage Reference, 5.0V Linear Voltage Regulator (LVR) and Power-on-Reset (POR). These cells are always powered on when the LINE\_IN voltage is applied and cannot be disabled. The Power Manager also contains a Voltage-to-Current Converter (VTOI) which sources current for use by all on-chip analog circuits. The VTOI reference is a precision external resistor connected to the REXT pin. In addition, a 1 $\mu$ A current is replicated and output at the IBIAS pin for use by the MuxCapacitor IC. The EN pin is used to disable the VTOI and Current Manifold for reduced power consumption during idle mode of operation.

The 5.0V LVR supplies the voltage for the Digital I/O on the Control IC and also supplies the VDDA supply voltage for the MuxCapacitor IC. A 10V LVR is also provided at the VREG10 pin to supply the voltage for the Forward Converter output driver connected to the FWDOUT pin.

The Control IC also provides the circuitry required to control an external Forward Converter using an Opto-Isolator feedback circuit. The analog Opto-Isolator input signal at the FWDIN pin is converted to a Pulse-Width-Modulated (PWM) signal to control an external MOSFET connected at the FWDOUT pin. Pulse-Width-Modulation is performed at a rate of 100KHz with a clock provided by the on-chip RC Oscillator.

The Digital Control Block provides logic for the configuration of the MuxCapacitor IC and control of the Forward Controller. The MCEN and MCCLK outputs provide the enable and clock for the MuxCapacitor IC. All clocks used on the Control IC are derived from the on-chip 200KHz Oscillator. This clock is divided down to 100KHz for the Forward Controller and to 1KHz for the MCCLK output. The Digital Control Block also contains a programmable timer for the Soft-Start control of the



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MuxCapacitor IC via the SOFSTRT pin. Testability logic is also provided for the Control IC and is controlled as a function of the TESTMD<2:0> input pins and the EXTRST pin.

The Control IC can be disabled using the EN input pin. When EN=0, the Control IC will be disabled and all analog and digital circuits are turned off.

### 5.2.1 Line-Side Bandgap Voltage and Current Reference Generator

The Control IC contains an ultra-low power Bandgap Reference Voltage and Current generator which is powered from LINE\_OP1. A temperature-compensated output voltage of 1.22V is provided for use as a reference by subsequent circuit blocks. The bandgap cell is self-starting at the application of the LINE\_IN voltage and is always powered on and cannot be disabled.

An optional external shunt Bandgap can be used in place of the internal Bandgap Voltage Reference. The external Bandgap device is connected to the BGEXT pin and is selected when the CTRLX pin is asserted 'high'. The required external Bandgap voltage is 1.25V.

### 5.2.2 5.0V Linear Voltage Regulator

The 5.0V Linear Voltage Regulator (LVR) is used to supply the voltage for the analog and digital circuits, and the I/O padding of the Control IC. The output of the Regulator is available at the VDDA pin to power the MuxCapacitor IC. An external 10 $\mu$ F capacitor must be connected between VDDA and ground for noise reduction.

The 5.0V LVR is always powered on at the application of the LINE\_IN voltage and cannot be disabled.

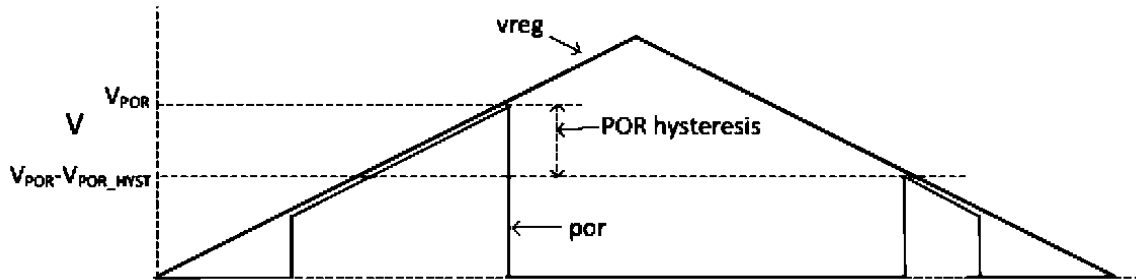
### 5.2.3 Power-on-Reset

The Power-on-Reset (POR) circuit monitors the internal VDDA supply voltage. For voltages at the VDDA pin less than the  $V_{POR}$  threshold voltage, the POR output will be asserted 'low' indicating a reset condition. For voltages at the VDDA pin greater than the  $V_{POR}$  threshold voltage, the POR output will be de-asserted 'high' for normal operation. Hysteresis is provided such that a reduction in the threshold voltage occurs once the  $V_{POR}$  threshold is exceeded. The reduced threshold with hysteresis now becomes  $V_{POR} - V_{HYS}$ .

An illustration of the operation of the power-on-reset block for a voltage ramp at the VDDA pin is shown below. The POR circuit is always powered on at the application of the LINE\_IN voltage and cannot be disabled.



**Figure 4: POR Threshold Voltages**



### 5.2.4 VTOI and Current Manifold

The Voltage-to-Current Converter (VTOI) produces a current referenced from an external precision resistor connected to the REXT pin. Using the Bandgap reference voltage, the VTOI generates a 0.5V bias at the REXT pin. With the connection of a 499K $\Omega$ , 1% resistor from REXT to ground, a precision 1 $\mu$ A current is generated. The Current Manifold uses this precision current to supply the bias currents to the analog circuits in the Control IC. A 1 $\mu$ A reference current is also output at the IBIAS pin for use by the MuxCapacitor IC.

### 5.2.5 Oscillator

The ultra-low power 200 KHz RC Oscillator produces the low-frequency clocks for the Control IC. The output of the oscillator is divided down to 100KHz for the Digital Control Block which provides clocks to the MuxCapacitor IC and the Forward PID Controller.

### 5.2.6 10V Linear Voltage Regulator

The 10V LVR provides the supply voltage for the Forward Converter output driver at the FWDOUT pin. The output of the 10V LVR is available at the VREG10 pin. An external 10 $\mu$ F capacitor must be connected between VREG10 and ground for noise reduction.

### 5.2.7 Forward PID Controller

The Forward PID Controller controls the external MOSFET of the Forward Converter using an opto-isolator feedback circuit. The feedback voltage signal is input at the FWDIN pin and is compared to the Bandgap voltage to generate an error voltage for the loop. The Error Amplifier creates a 3<sup>rd</sup> order compensation network with on-chip passive components. The resulting transfer function of the PID Feedback Loop is comprised of 2 poles and 2 zeros to ensure that the regulator output is stable for the full range of load conditions.



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The two zeroes provide 180 degree of phase boost in order to negate the 180 degree of phase loss due to the output LC filter. Both zeroes are placed at 50% of the LC filter pole frequency. The two poles are located at the switching frequency of the converter (100KHz). The Forward PID Feedback Loop uses Pulse-Width Modulation (PWM) to control the amount of time the external MOSFET switch is turned 'on' to supply current to the load. This is achieved with a comparator which receives the output of the Error Amplifier and compares it to the sawtooth waveform output of the Sawtooth Generator. The 100 KHz clock provided by the Digital Control Block is used by the Sawtooth Generator to develop the sawtooth input to the Comparator.

### 5.2.8 Country Selector

The Country Selector uses the scaled LINE\_IN voltage at LINE\_OP1 to determine the appropriate gain (or divider ratio) for the MuxCapacitor stages of the MuxCapacitor IC. The scaled LINE\_IN voltage is compared to the Bandgap reference voltage to output one of the possible gain settings as a function of the AC Mains voltage. The outputs of the Country Selector are input to the Digital Control Block to decode the appropriate gain setting required by the MuxCapacitor IC.

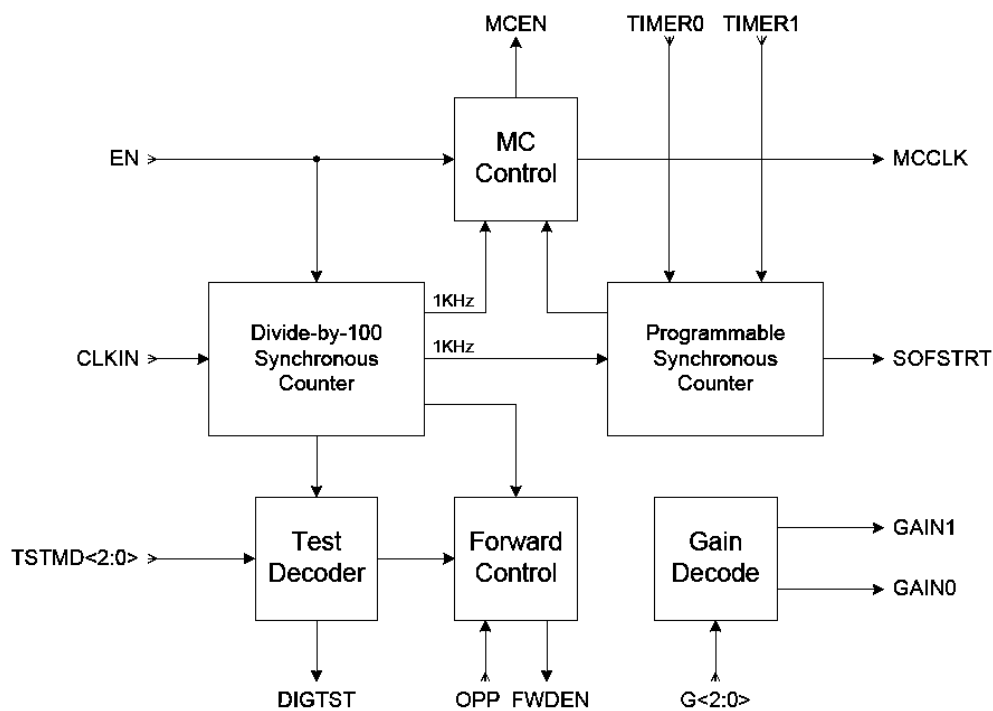
### 5.2.9 Over-Current Protection

Overcurrent protection for the Forward Converter is achieved by sensing the current flowing through the external switching MOSFET and the primary winding of the transformer. The voltage developed across the external current sense resistor is placed in series with the MOSFET and transformer is applied to the pin RCSP. This RCSP voltage is compared to a reference voltage. When an over-current condition is detected the Forward PID Controller is disabled and the DIGTST output pin will be asserted 'high'. The Forward PID Controller will remain disabled until the TSTMD2 input is momentarily asserted 'high'. Then the Forward Converter operation will be restored.

### 5.3 Digital Control Block

The Digital Control Block provides the logic control and configuration of the MuxCapacitor IC as well as control of the Forward PID Controller. The block diagram of the Digital Control Block is shown below.

**Figure 5: Digital Control Block Diagram**



All clocks used in the Control IC are derived from the on-chip Oscillator which is divided down by a 5-bit synchronous counter to create the 1KHz for the MCCLK output. The 1KHz output of the counter is also used for the programmable Soft-Start timer for the SOFSTRT pin. The Soft-Start timer is programmable to one of four possible timeout values using the TIMER0 and TIMER1 input pins as shown below.



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**Table 18: Soft-Start Timer Program Settings**

TIMER1	TIMER0	SOFSTR Timeout (mS)
0	0	10
0	1	30
1	0	20
1	1	40

The Gain Decode block receives the Country Selector outputs and creates the GAIN0 and GAIN1 outputs to control the MuxCapacitor IC gain setting

The Forward Control block provides the enable for the Forward PID Controller and also disables the block when an over-current detection is detected at the *OPP* input of the RCSP pin. Following the over-current event detection, the *OPP* signal is reset by the assertion of the TSTMD<2> input pin.

Logic is also provided for testing the Control IC as a function of the TESTMD<2:0> input pins and the EXTRST pin. When the EXTRST pin is asserted 'high' all of the digital logic is reset overriding the internal Power-on-Reset. The three TSTMD inputs provide access to internal analog and digital signals through the use of digital and analog multiplexers. Internal digital signals can be multiplexed to the DIGTST output and internal analog signals can be multiplexed to the ANATST pin. The truth table for the digital test mode inputs is shown below.

**Table 19: Test Select Truth Table**

Test Select Input Pins			Function
TSTMD2	TSTMD1	TSTMD0	
0	0	0	DIGTST = Over-Current Detect Output
0	0	1	DIGTST = Forward Clamp Comparator
0	1	0	DIGTST = Forward Softstart OK
0	1	1	DIGTST = 100KHz Oscillator Output
1	0	0	Reset Over-Current Detection
1	0	1	Disable Forward PID Controller
1	1	0	ANATST = Bandgap Voltage
1	1	1	Logic Test Mode



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When  $TSTMD\langle 2:0 \rangle = 3'b111$ , the Logic Test Mode is enabled. This allows an external clock to be input at the CTRLX pin bypassing the on-chip oscillator. A higher-speed clock can be used to test the digital logic reducing the test time.

The digital inputs of the Control IC are configured as a NAND-Tree allowing the inputs to be tested at wafer probe or package test. When the EXTRST pin is asserted 'high' the NAND-Tree is enabled with the output muxed to the MCEN output pin. The test begins with all inputs asserted 'high' as shown below. They are sequentially taken 'low' in the order shown in the table.

**Table 20: NAND-Tree Test Sequence**

CTRLX	TSTMD2	TSTMD1	TSTMD0	EN	TIMER1	TIMER0	MCEN
1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	0
1	0	1	1	1	1	1	0
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	0	1	0
1	1	1	1	1	1	0	0



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### 6 Reference System Application

The following system diagram provides a 10W application schematic for a 5.0V output. The HS100 chip-set is combined with a Forward Converter delivering the specified efficiency for a load of 50mA to 2.0A. In this configuration the MuxCapacitor stages of the MuxCapacitor IC are connected in parallel to deliver 100mA at the input to the transformer primary.

Other configurations are possible including World-wide applications.

The electrical characteristics of the HS100 Reference System are summarized.

**Table 21: HS100 System Characteristics**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>AC</sub>	AC Input Voltage	US-only operation	108	120	132	VAC
		World-wide operation	90		240	
V <sub>LINE_IN</sub>	DC Line Voltage	US-only operation	152	170	187	VDC
		World-wide operation	127		340	
F <sub>in</sub>	Input Frequency		47		63	Hz
V <sub>PRIM</sub>	Primary Voltage			110		V
Q <sub>ir</sub>	In-Rush charge				TBD	Coulombs
V <sub>o</sub>	Output Voltage	Average voltage	4.75	5.0	5.25	Vdc
I <sub>o</sub>	Output Current		0		2.0	A
P <sub>OUT</sub>	Output Power				10	W
V <sub>oa</sub>	Output Accuracy		-5.0		+5.0	%
VR	Voltage Regulation	50mA ≤ I <sub>LOAD</sub> ≤ 2.0A			TBD	%
V <sub>RIPPLE</sub>	Output Voltage Ripple		-2		+2	%
V <sub>td</sub>	Voltage Temp drift				TBD	% / °C
EF <sub>fl</sub>	Efficiency, Full Load	P <sub>out</sub> /P <sub>in</sub>	95			%
EF <sub>ll</sub>	Efficiency, Light Load	P <sub>out</sub> /P <sub>in</sub>	92			%
P <sub>nl</sub>	No Load Power Output				10	mW

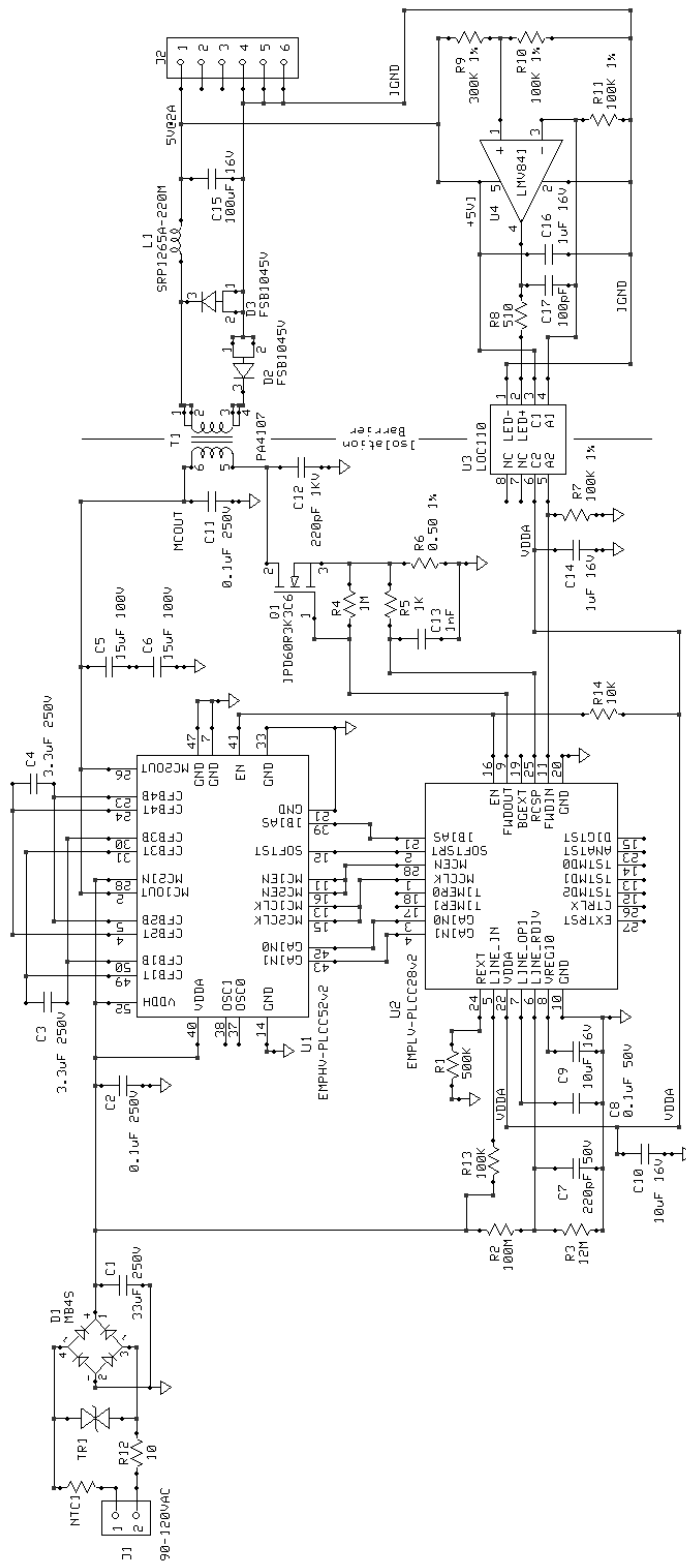


Figure 6: HS100 Japan/USA Application Schematic

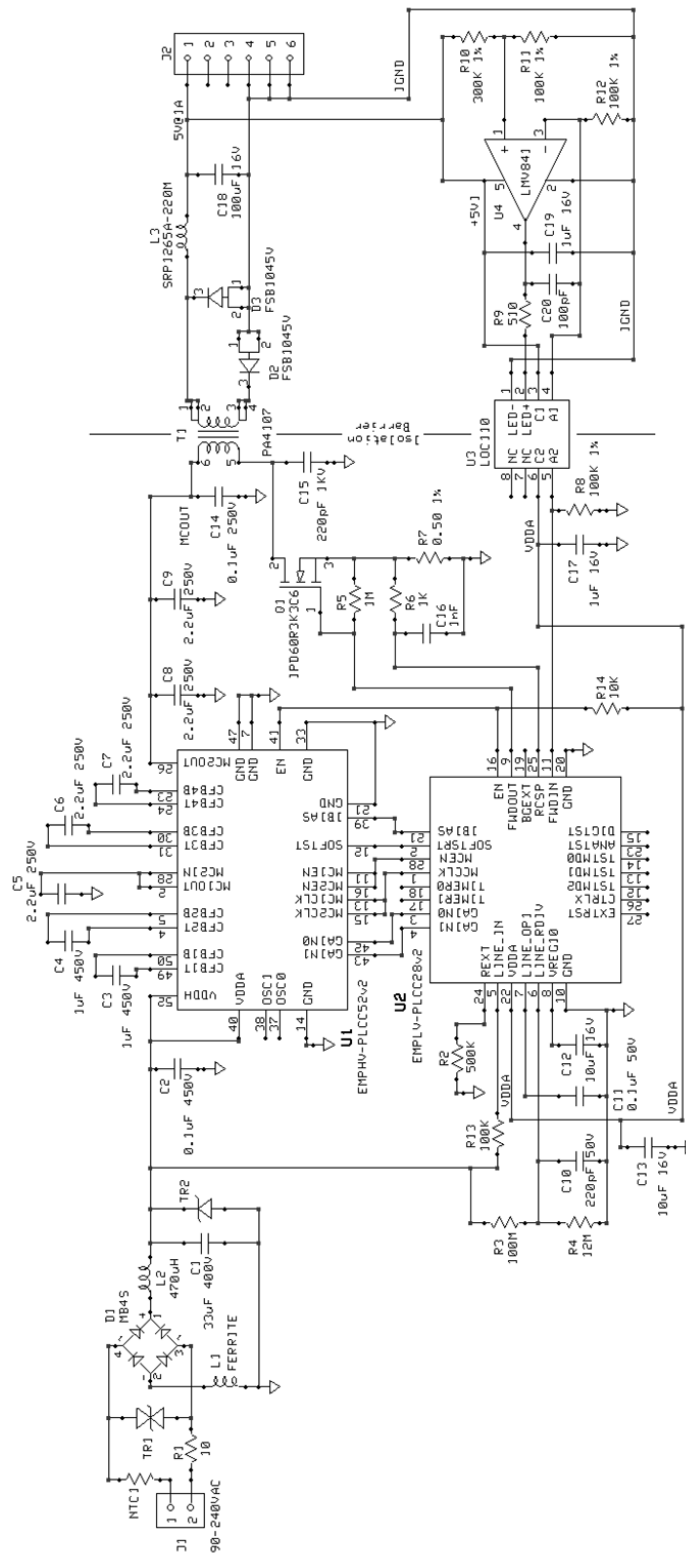


Figure 7: HS100 Universal Application Schematic



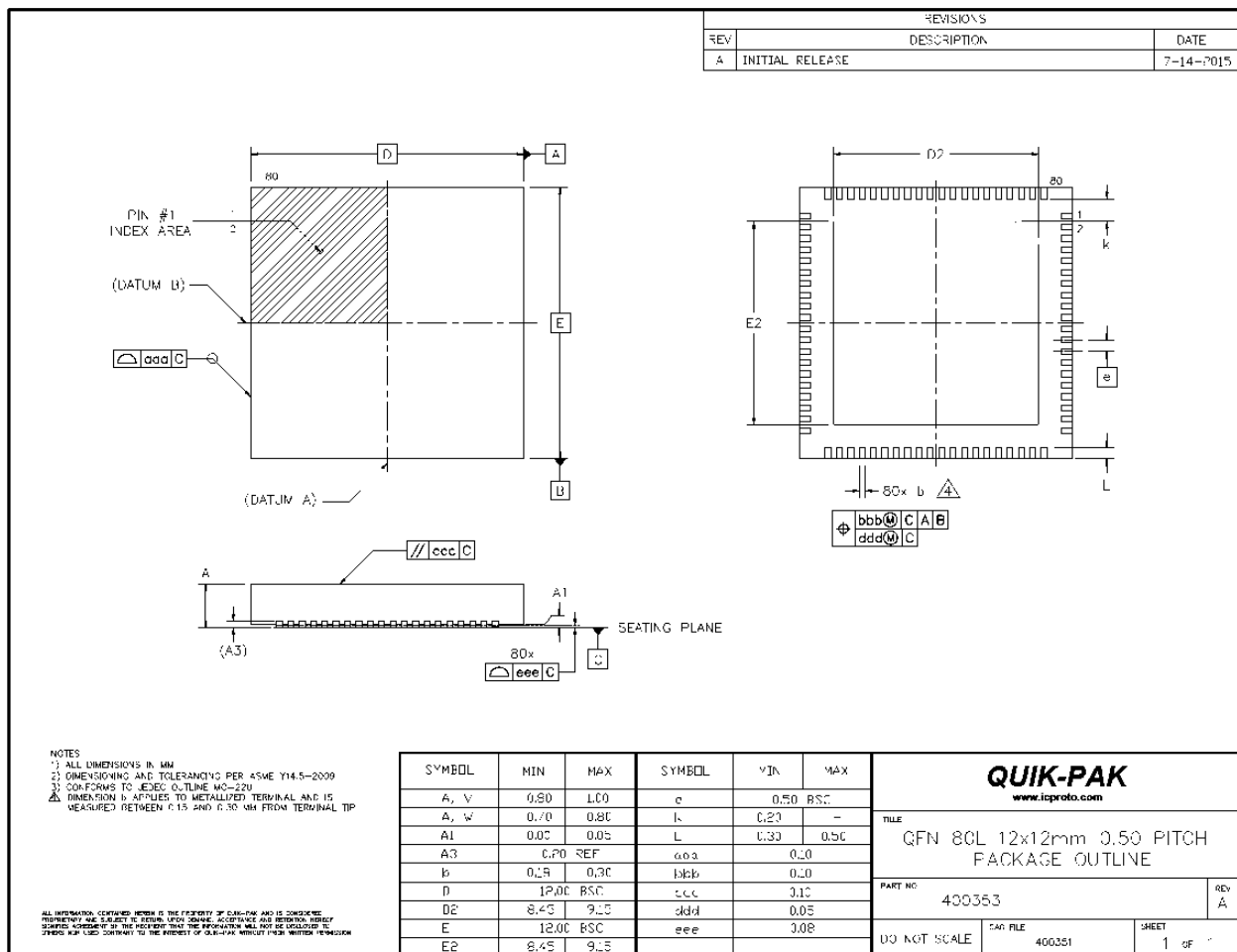
### 7 Package Drawings

The packages for the HS100 MuxCapacitor and Control IC's are shown in the following drawings.

#### 7.1 MuxCapacitor IC

The HS100 MuxCapacitor IC is packaged in a 80-pin QFN package as shown below.

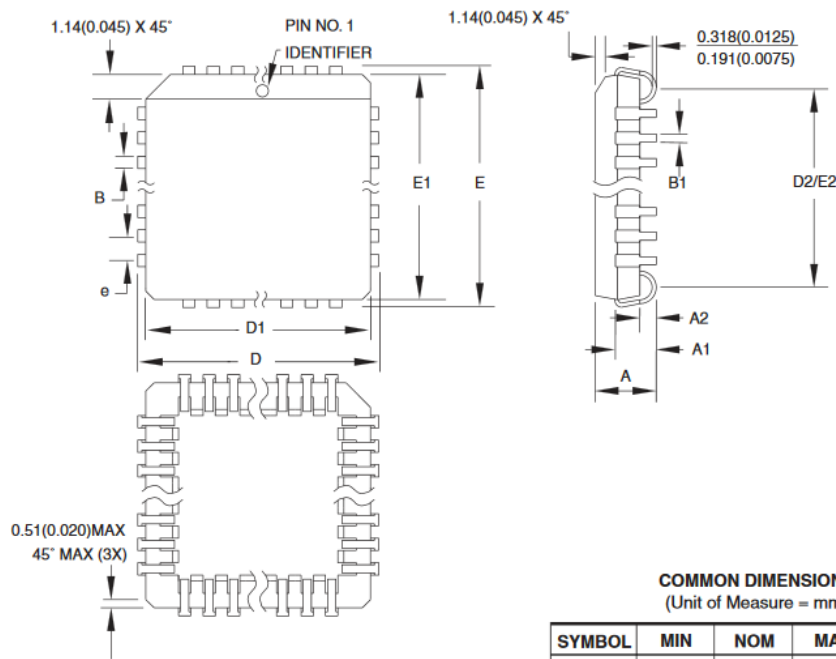
**Figure 8: HS100 MuxCapacitor IC Package Drawing**



### 7.2 Control IC

The HS100 Control Low-Voltage IC is packaged in a 28-pin PLCC package as shown below.

**Figure 9: HS100 Control IC Package Drawing**



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	-	4.572	
A1	2.286	-	3.048	
A2	0.508	-	-	
D	12.319	-	12.573	
D1	11.430	-	11.582	Note 2
E	12.319	-	12.573	
E1	11.430	-	11.582	Note 2
D2/E2	9.906	-	10.922	
B	0.660	-	0.813	
B1	0.330	-	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AB.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.



# Helix Semiconductors

## HS100 Data Sheet

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**Table 22: Revision History**

Date	Revision	Description
3.15.17	1	Initial Release

### Headquarters

9980 Irvine Center Drive  
Suite 100  
Irvine, CA 92618

### Information & Sales

949-748-6057  
sales@helixsemiconductors.com

### Technical Support

949-748-7026  
support@helixsemiconductors.com

### Regional Office

5475 Mark Dabling Blvd.  
Suite 206  
Colorado Springs, CO 80918

949-748-6057  
designs@helixsemiconductors.com